Amendments to the Specification

Kindly amend paragraph [0038] as follows:

[0038] FIG. 2 depicts an intermediate structure in a semiconductor processing approach in accordance with the present invention. This structure, generally denoted 100, again includes a substrate 102, such as a silicon substrate having isolation regions 104 between which gate stacks are to be defined. Although not shown, device NFET/PFET/array well implants are assumed to have taken place. A gate oxide 106 has been formed and patterned above which blanket uncapped intrinsic polysilicon 108 has been formed and patterned employing a photo resist mask 110. If the memory cell comprises a trench capacitor, then the trench process has been completed. If the memory cell is stacked, then the process sequence will integrate with the back end of line (BEOL) processings. In either scenario, the storage device is independent of the concepts presented. The process action carried out in FIG. 2 is to pattern the polysilicon gates. Note that the array bit-line space between gate stacks is again a minimum image. As used herein, the "first contact hole" refers to the region in FIG. 2 defined by the top of the polysilicon film (108) to the substrate (102), and resulting from the gate patterning step.

Kindly amend paragraph [0042] as follows:

[0042] FIG. 5 depicts one field effect transistor of structure 100, wherein a hard mask 130 (e.g., TEOS oxide) has been deposited and patterned to define an opening 132 exposing source/drain implant 116 above which the bit-line contact is to be formed. The photo resist mask 130 is assumed to land somewhere over the gate 108 and etching of the mask and oxide/nitride layers proceeds until a portion of the polysilicon gate 108 is exposed. As used herein, the "second contact hole" includes the region in FIG. 5 defined above the top of polysilicon film (108) to the top of the dielectric layer (122) and above. As shown in FIG. 5, the second contact hole extends over the first contact hole and exposes a portion of the top, horizontal surface of the gate structure.